K4HJU

Amateur Radio
Woodcreek, Texas

JRS Frequency Counter 1972 Restoration/ Rejuvenation

Rev 0.00
Jim Satterwhite “Satter” K4HJU

A Work in Progress

K4HJU
1/25/2018

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1. Introduction

In 1972 I began the design of a battery operated frequency counter as a lunch hour project at Bell Labs. At the time we were doing field work developing a test set for "outside - in" fault location in buried telephone cables. This required measurements in the field and we didn't have a suitable battery operated frequency counter. I made a deal with my supervisor that I would design such a counter on my lunch hour and I would get to keep my prototype and one of the production models. I enjoyed the design and development. Fortunately or unfortunately, just as we were finishing the project HP released their 5380 series battery operated frequency counters. At that time we (Jerome Parker and I) had completed the design and built a few models. Since then this frequency counter has been my "go to" frequency counter in my lab. I have five other more modern frequency counters in lab and this counter is still my "go-to" counter for most things.

Recently, it failed and I went in to it to repair it. I found that a transistor in the front end had failed and I replaced it; however in the process I had inadvertently broken something else. Although, I had near current schematics that fault was very difficult to locate. Jerry (Jerome) the mechanical engineer had decided to use "cordwood" construction for the modules similar to that used in the Sprint/Spartan missile guidance sets we had been working on previously. With integrated circuits, cordwood construction is a nightmare from a construction and maintenance point of view. With that and the fact, although I had schematics that reflected my breadboard and the essence of the final design, I did not have the wiring layout.

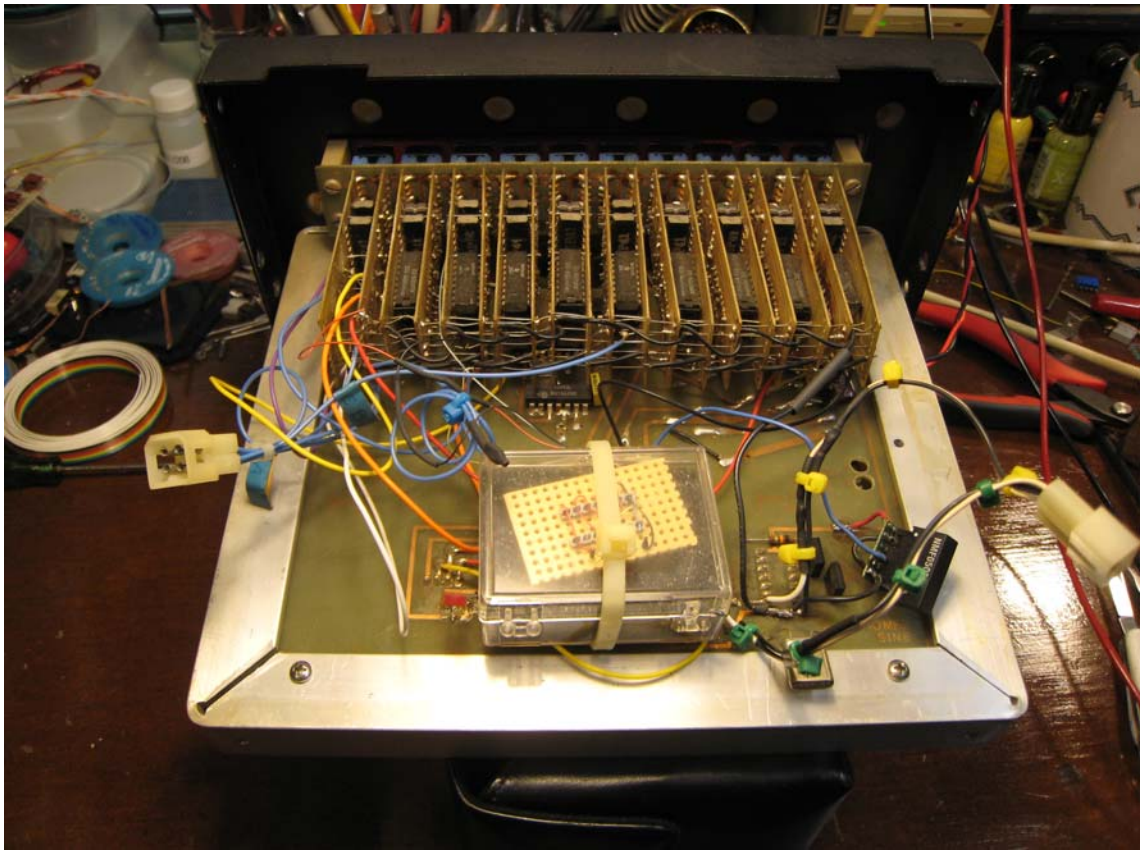

Figure 1-1 Top side of Counter

Figure 1-1 shows the top side of the counter with the display modules. In addition there is the plastic box containing a previous "fix" to one of the display modules.

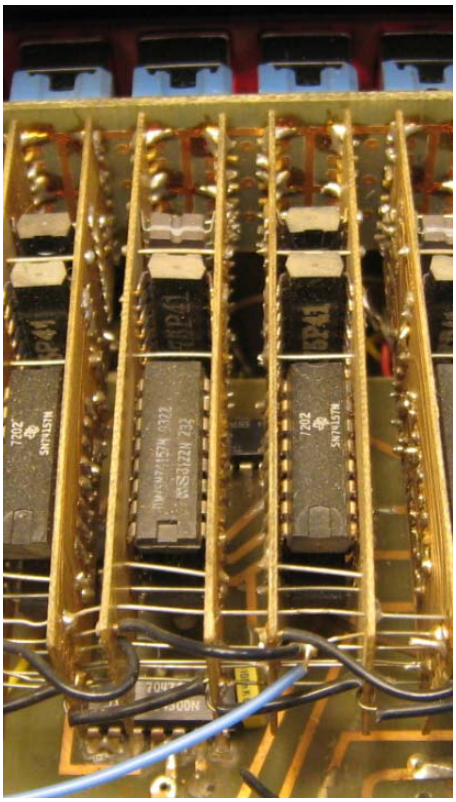

Figure 1-2 Display module cordwood construction

Figure 1-2 shows the cordwood construction of the display modules. Maintenance of this construction nearly impossible. In this construction the IC pins are bent outward from the chip and the leads are aligned and fed through PCBs on both sides. This is a very, very tedious alignment problem. In addition, there is no way to replace an IC if it fails or there is an error. How Jerry actually constructed these modules remains a mystery to me. To date only one chip in one module has failed and I was able to jumper around that with an external circuit.

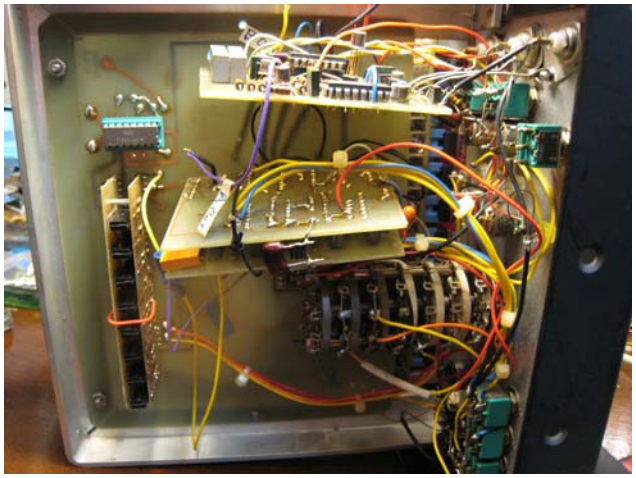

Figure 1-3 Bottom view of counter

Figure 1-3 shows the bottom view of the counter. With no wiring diagram for the modules or the chassis, maintenance is very difficult, particularly with the modules in place.

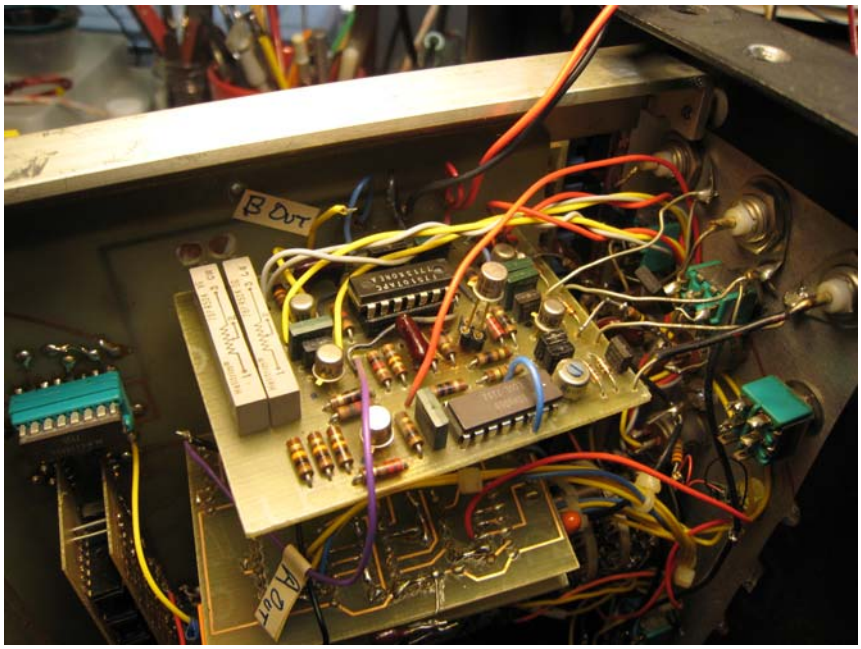

Figure 1-4 Example of wiring

As I was recovering from a serious illness and had some time on my hands, I decided to rebuild the counter and clean up the wiring.

2. Design

The original design is done with 7400 series TTL logic chips, therefore very power hungry.

3. Rebuild

I decided to rebuild the counter using the old cordwood modules. I added sockets to the modules on the main chassis. To determine the wiring required reverse engineering the counter. I created schematics of the modules and the wiring. I then took it apart and began the rebuild, connectorizing every separate assembly. I removed the crystal oscillator circuit and replaced it with a high stability oven controlled crystal oscillator.

The original design used a high speed decade counter for the first stage employing 74S00 series logic. I replaced this with a decade counter employing 74HCxx series logic..

Insulation displacement wiring was used to interconnect the circuits on the mother board.

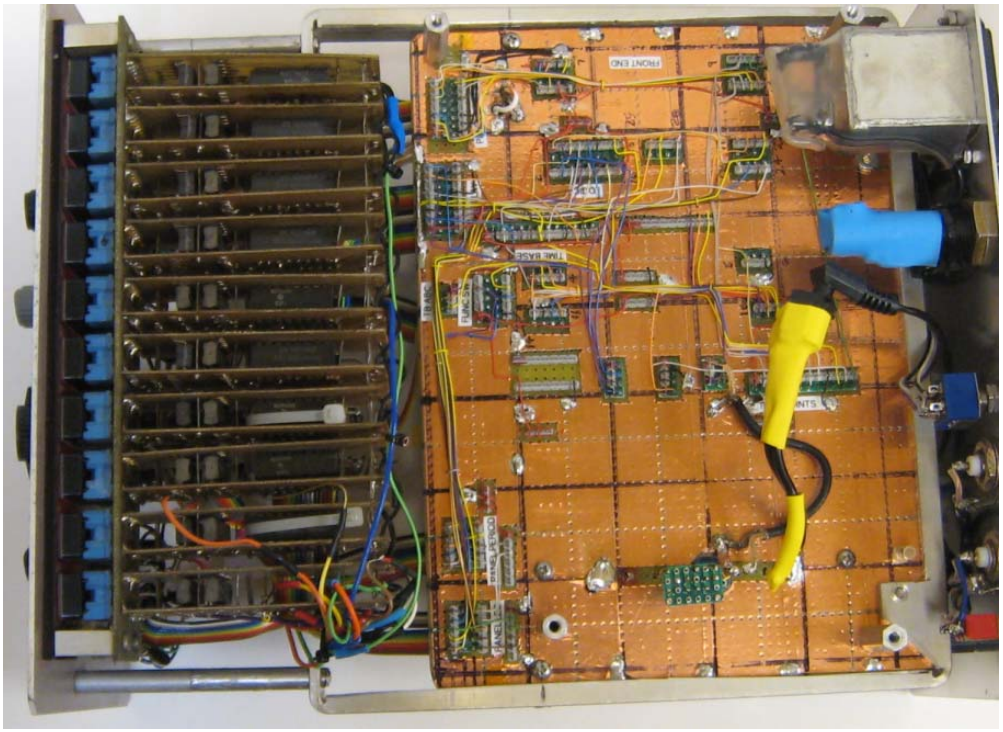

Figure 3-1 Top view

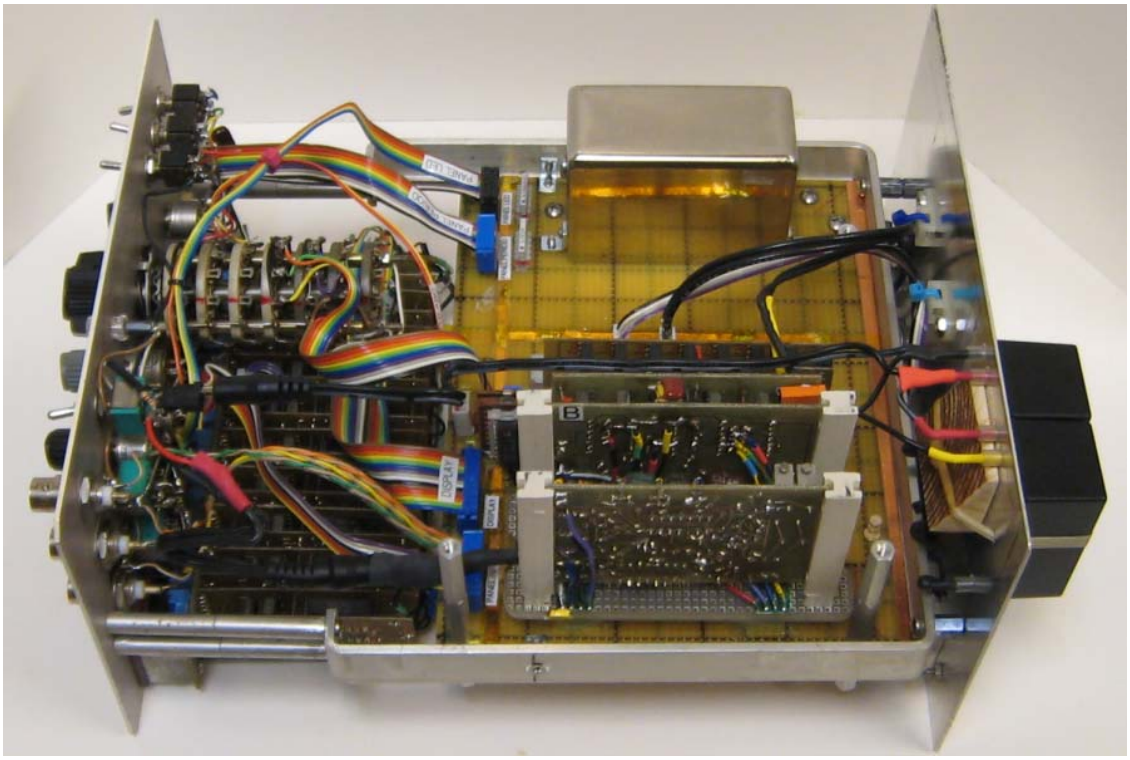

Figure 3-2 Bottom view

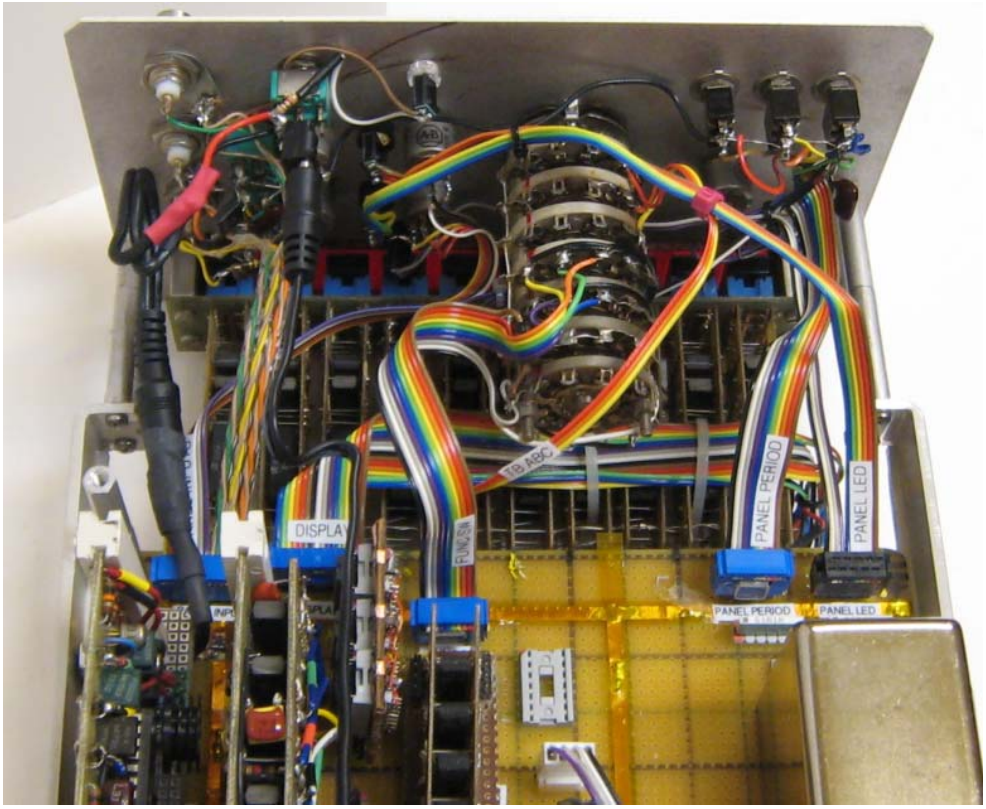

Figure 3-3 Front Panel wiring

Figure 3-4 The Rejuvenated Counter in It's New Case

4. References

- J. R. Satterwhite, "A Battery-Operated Digital Frequency Counter and Time Interval Instrument", October 18, 1972, Bell Laboratories Memorandum for File

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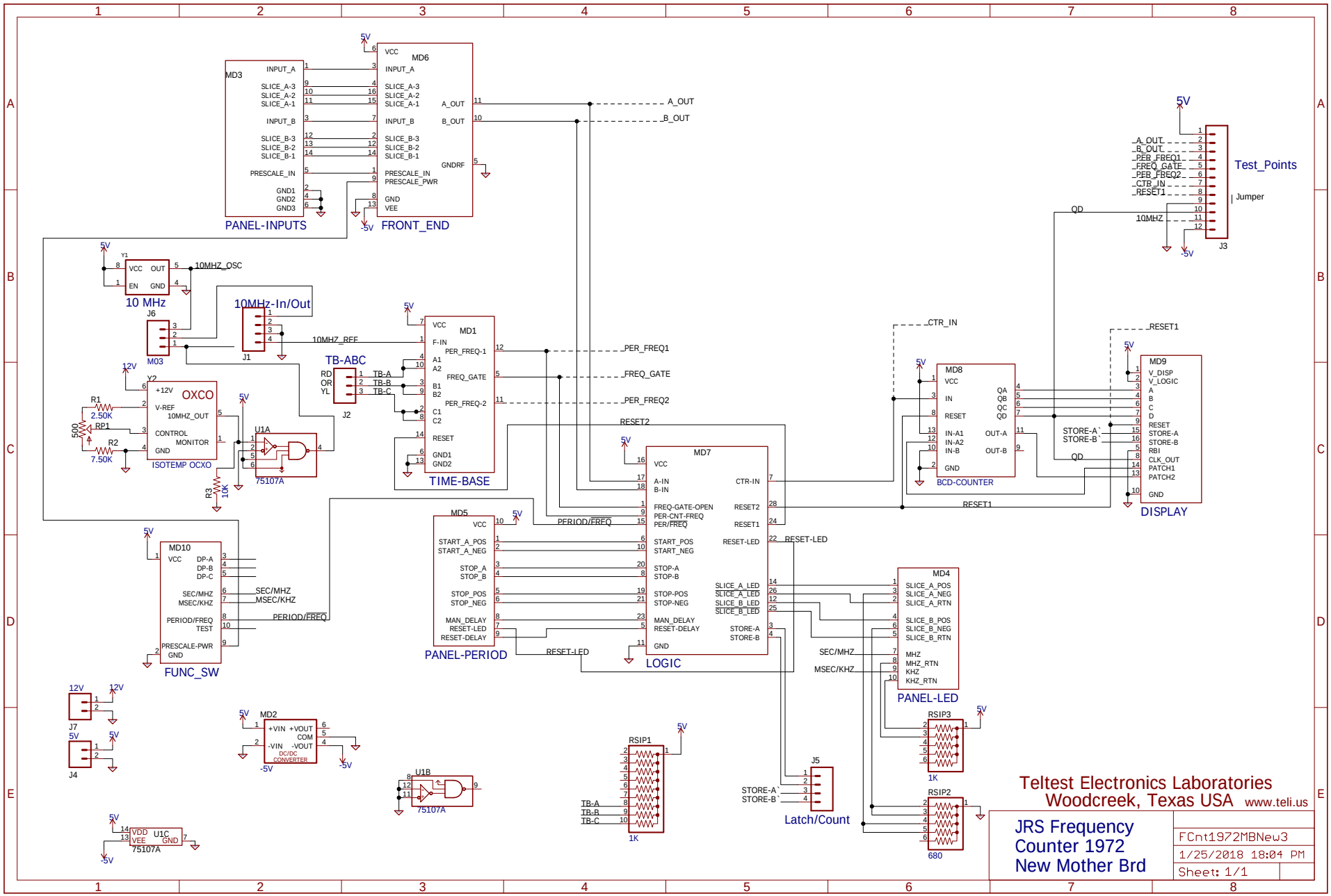
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MD6
PANEL-INPUTS
FRONT_END
A_OUT
B_OUT
Test_Points
Jumper
J3
10 MHz
10MHz-In/Out
J6
M03
J1
10MHZ_OSC
10MHZ_REF
TB-ABC
J2
TB-A
TB-B
TB-C
OXCO
ISOTEMP OCXO
R1
2.50K
RP1
500
R2
7.50K
R3
10K
U1A
75107A
MD1
TIME-BASE
PER_FREQ1
FREQ_GATE
PER_FREQ2
RESET2
CTR_IN
RESET1
MD8
BCD-COUNTER
MD9
DISPLAY
MD7
LOGIC
MD5
PANEL-PERIOD
PERIOD/FREQ
RESET-LED
MD10
FUNC_SW
SEC/MHZ
MSEC/KHZ
MD4
PANEL-LED
MD2
DC/DC CONVERTER
U1B
U1C
RSIP1
RSIP2
RSIP3
1K
680
J5
Latch/Count
STORE-A`
STORE-B`
J7
J4
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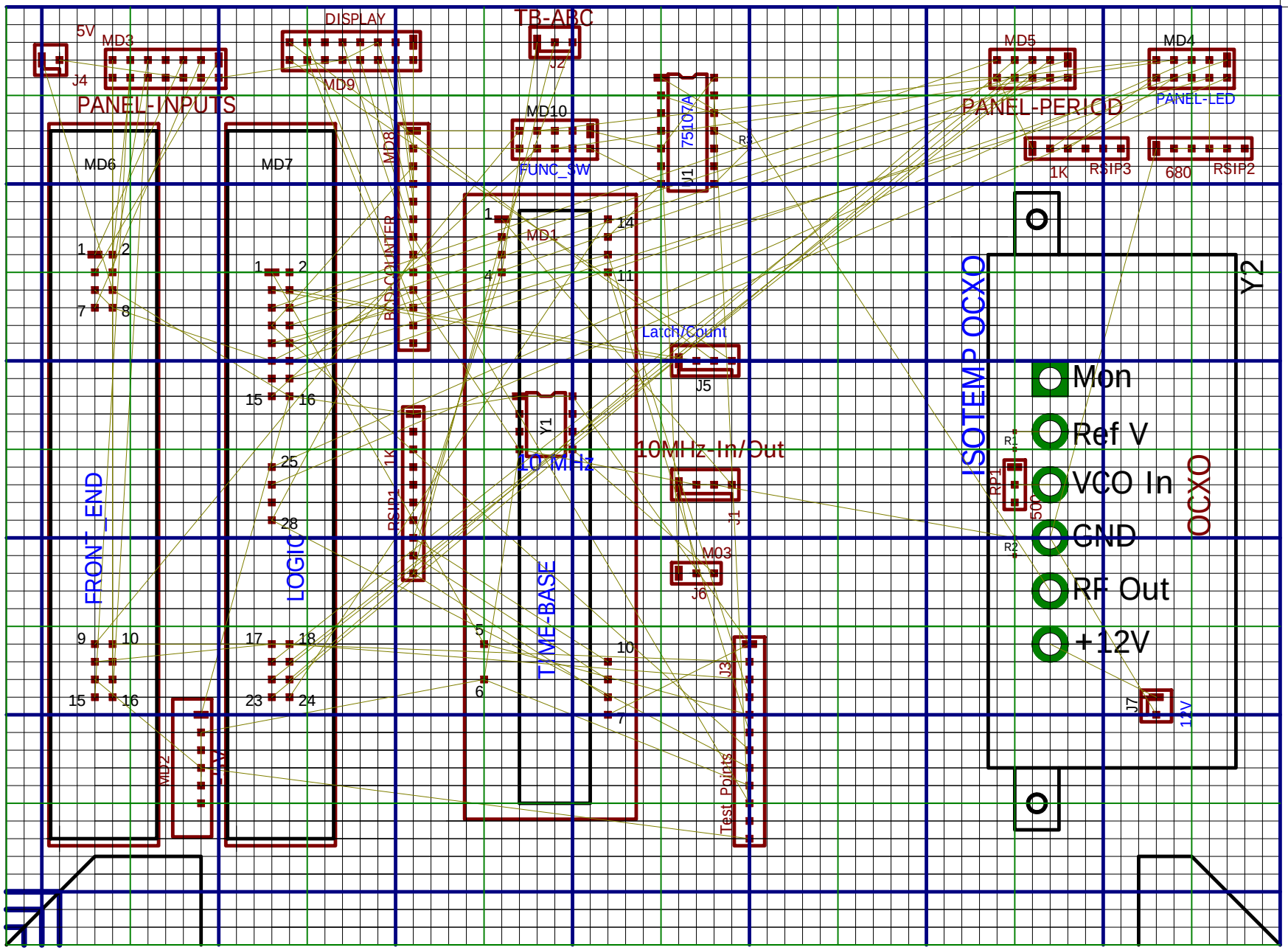
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DISPLAY
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TB-ARC
J2
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75107A
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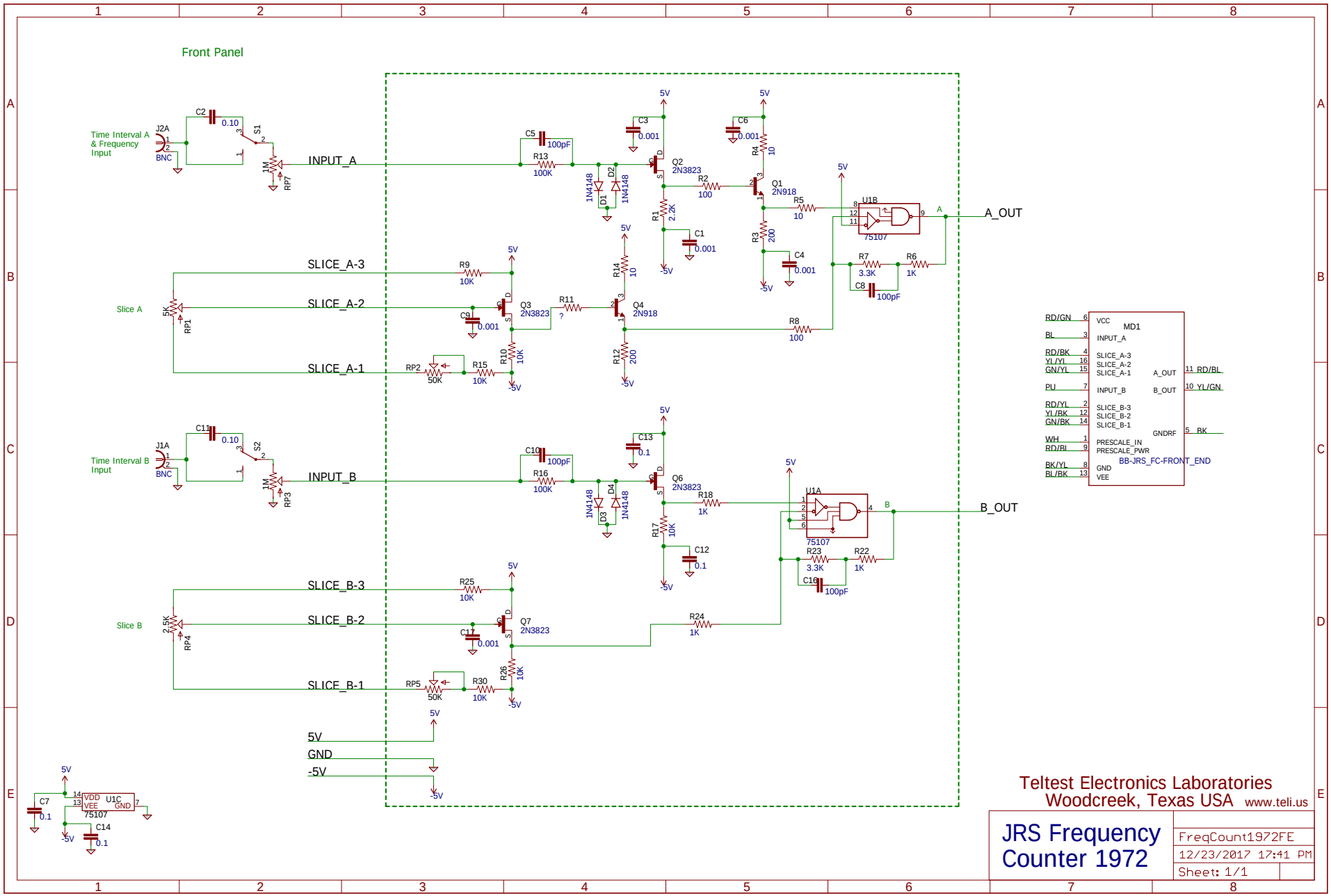
R3
MD5
MD4
PANEL-PERIOD
PANEL-LED
1K
RSIP3
680
RSIP2
MD6
MD7
MD8
BCD-COUNTER
MD1
U1
Latch/Count
J5
Y1
10 MHz
10MHz-In/Out
J1
RSIP1
1K
MD03
J6
FRONT_END
LOGIC
TIME-BASE
J3
Test Points
MD2
J7
12V
ISOTEMP OCXO
Y2
OCXO
Mon
Ref V
VCO In
GND
RF Out
+12V
R1
RP1
50
R2


Front Panel
Time Interval A & Frequency Input
Time Interval B Input
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INPUT_B
A_OUT
B_OUT
SLICE_A-3
SLICE_A-2
SLICE_A-1
SLICE_B-3
SLICE_B-2
SLICE_B-1
Slice A
Slice B
5V
GND
-5V
Q1 2N918
Q2 2N3823
Q3 2N3823
Q4 2N918
Q6 2N3823
Q7 2N3823
U1A
U1B
U1C
75107
MD1
BB-JRS_FC-FRONT_END
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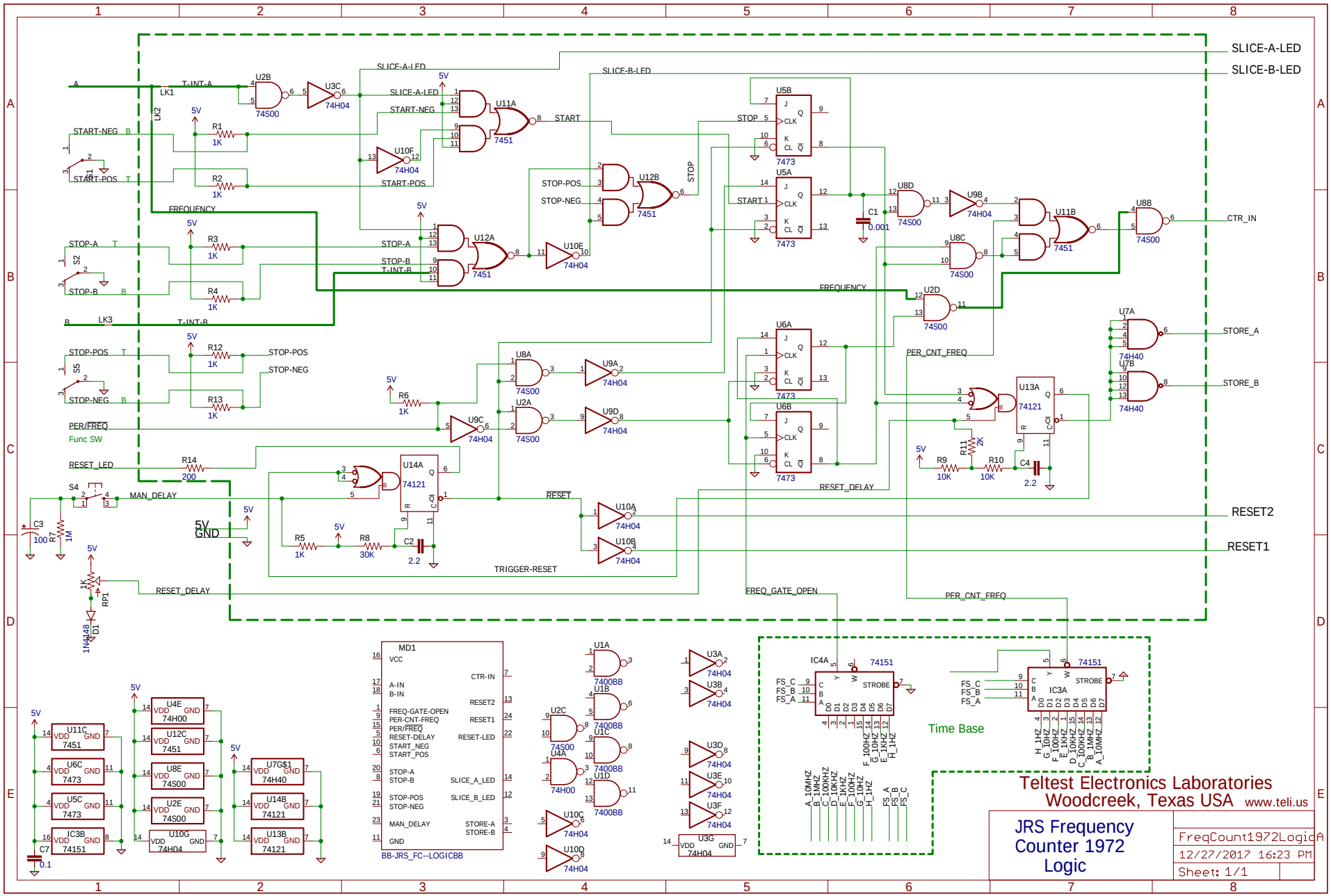
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SLICE-B-LED
CTR_IN
STORE_A
STORE_B
RESET2
RESET1
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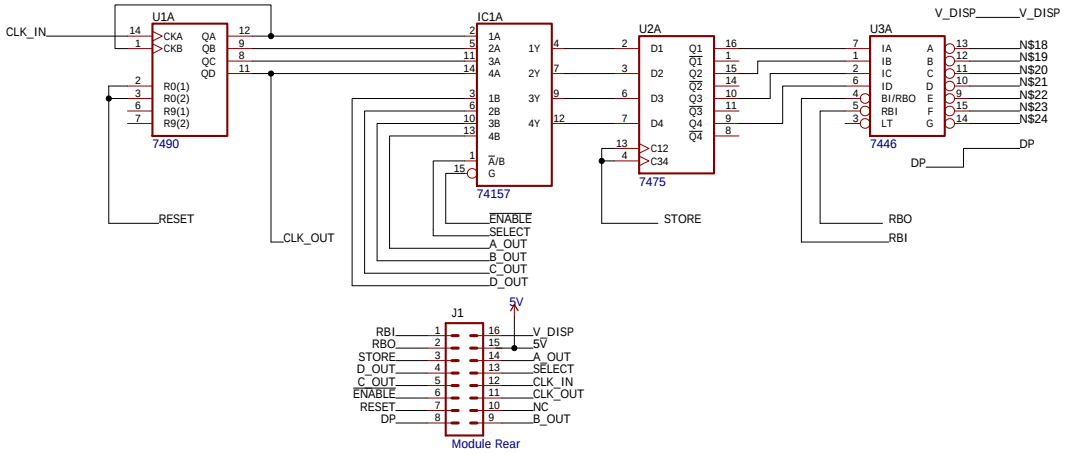
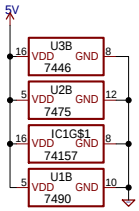
Time Base





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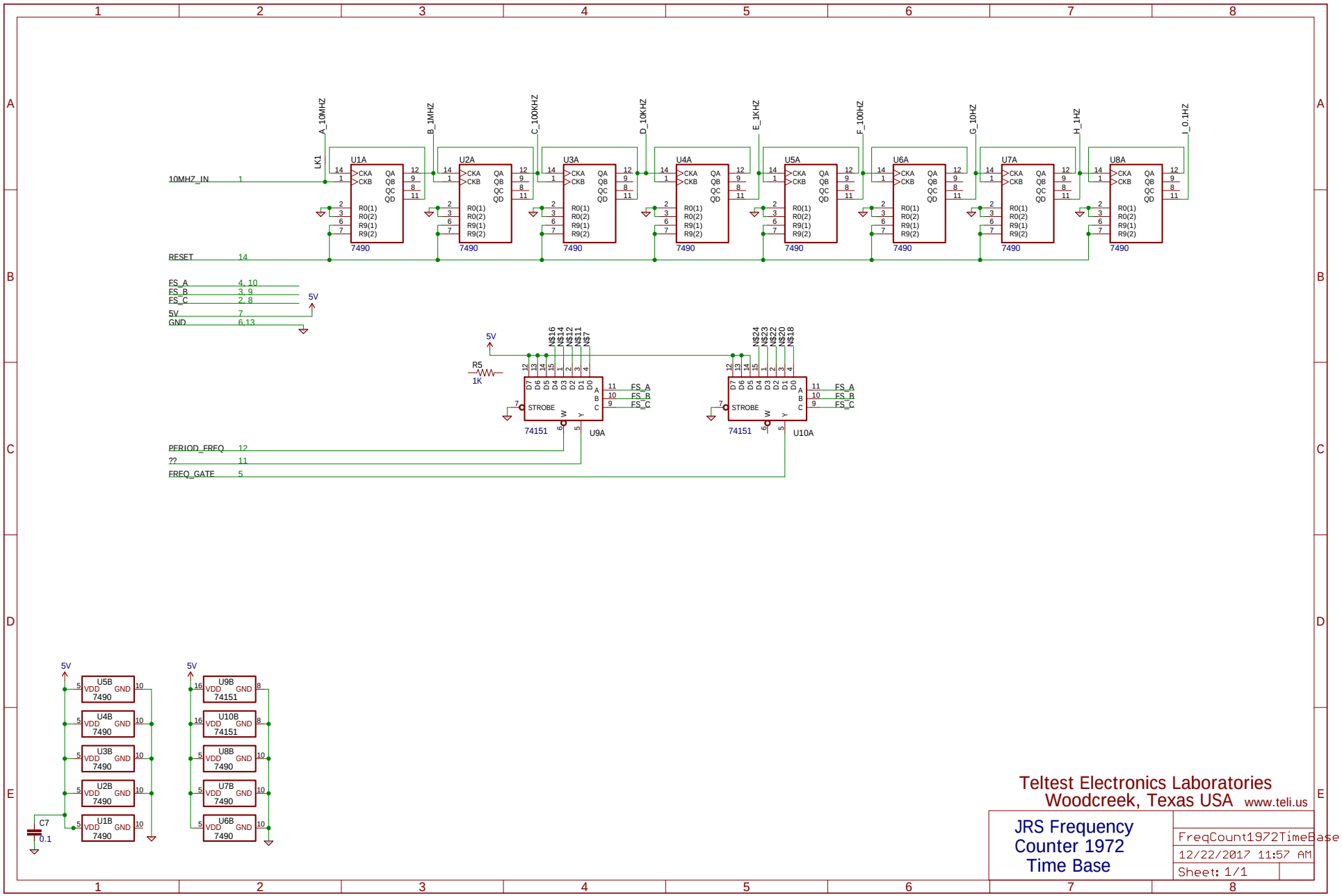
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F_100HZ
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I_0.1HZ
LK1
U1A
U2A
U3A
U4A
U5A
U6A
U7A
U8A
7490
10MHZ_IN 1
RESET 14
FS_A 4, 10
FS_B 3, 9
FS_C 2, 8
5V 7
GND 6,13
R5
1K
74151
U9A
U10A
PERIOD_FREQ 12
?? 11
FREQ_GATE 5
U5B
U4B
U3B
U2B
U1B
U9B
U10B
U8B
U7B
U6B
C7
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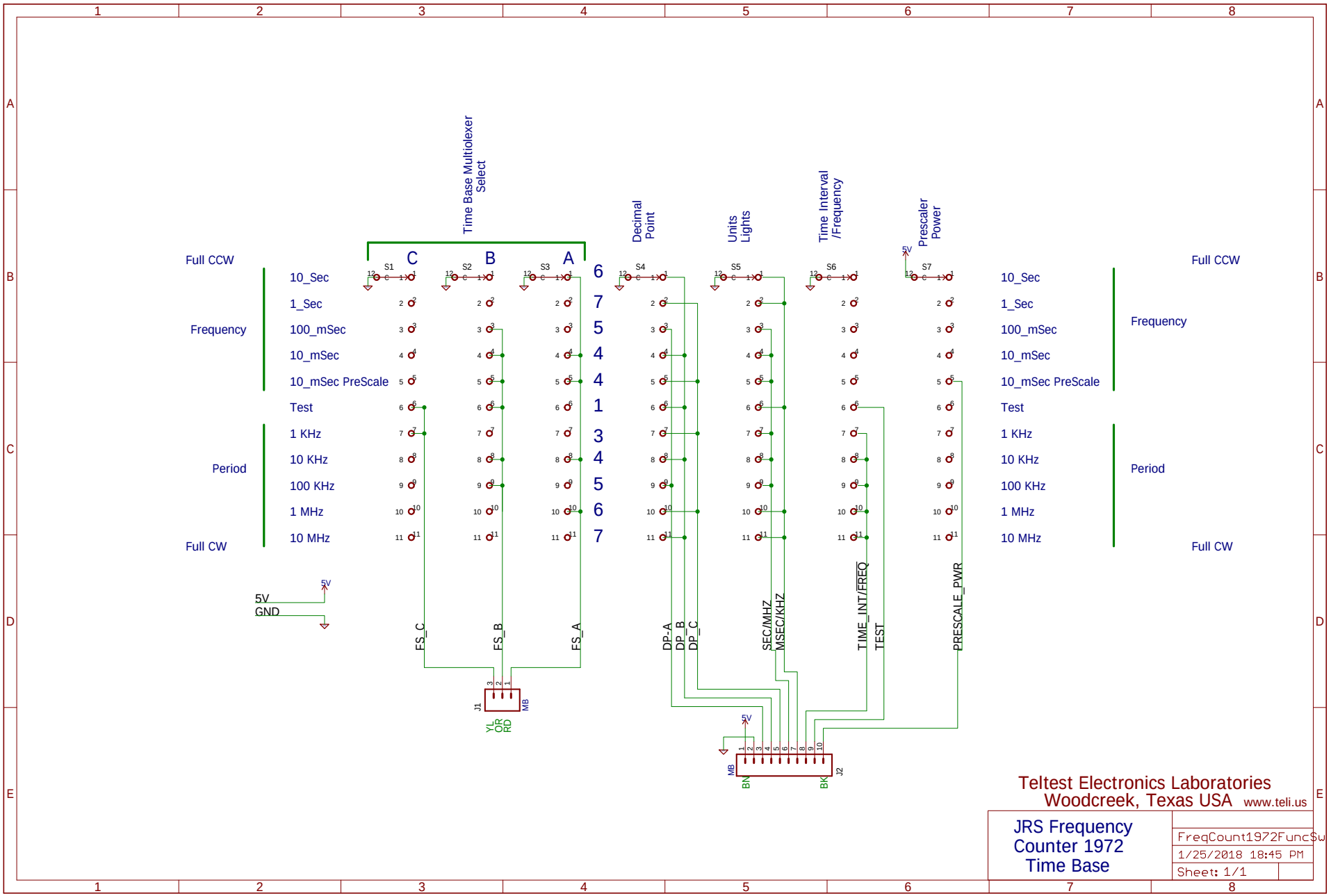
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C
B
A
Decimal Point
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Time Interval /Frequency
Prescaler Power
Full CCW
Frequency
10_Sec
1_Sec
100_mSec
10_mSec
10_mSec PreScale
Test
Period
1 KHz
10 KHz
100 KHz
1 MHz
10 MHz
Full CW
S1
S2
S3
S4
S5
S6
S7
5V
GND
FS_C
FS_B
FS_A
DP-A
DP_B
DP_C
SEC/MHZ
MSEC/KHZ
TIME_INT/FREQ
TEST
PRESCALE_PWR
J1
J2
MB
YL
OR
RD
BN
BK
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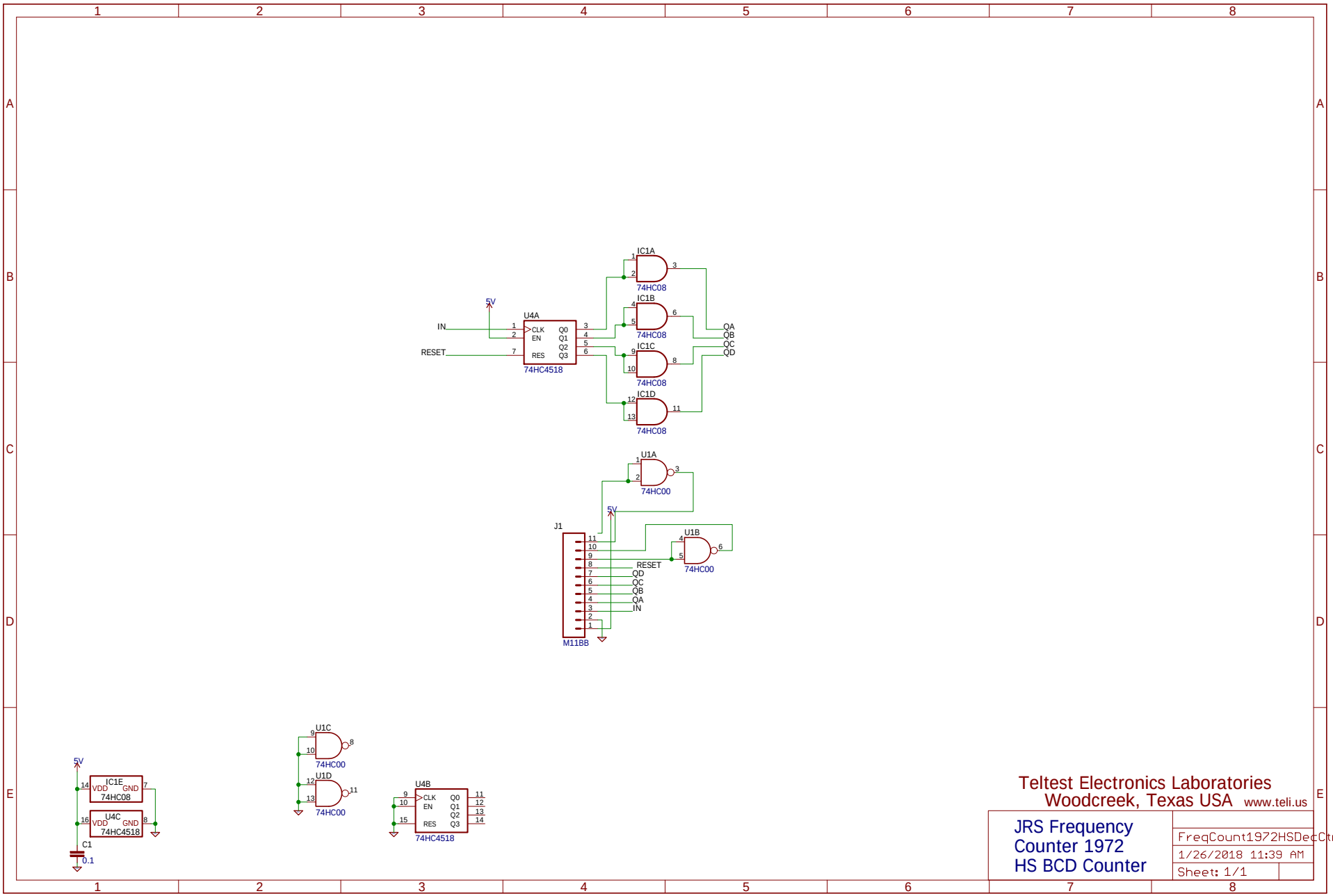
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6
7
8
A
B
C
D
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IC1C
74HC08
IC1D
74HC08
5V
U4A
IN
RESET
CLK
EN
RES
Q0
Q1
Q2
Q3
74HC4518
QA
QB
QC
QD
U1A
74HC00
J1
M11BB
U1B
74HC00
RESET
QD
QC
QB
QA
IN
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IC1E
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U4C
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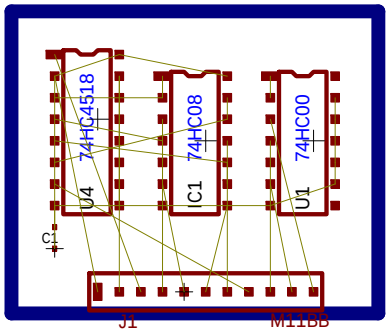
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J1
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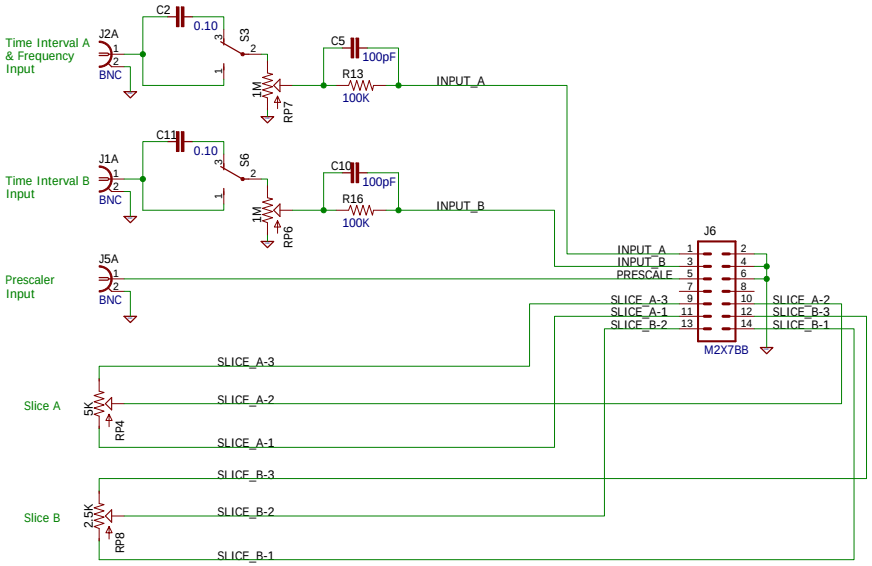

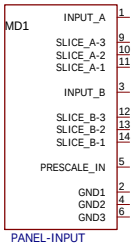

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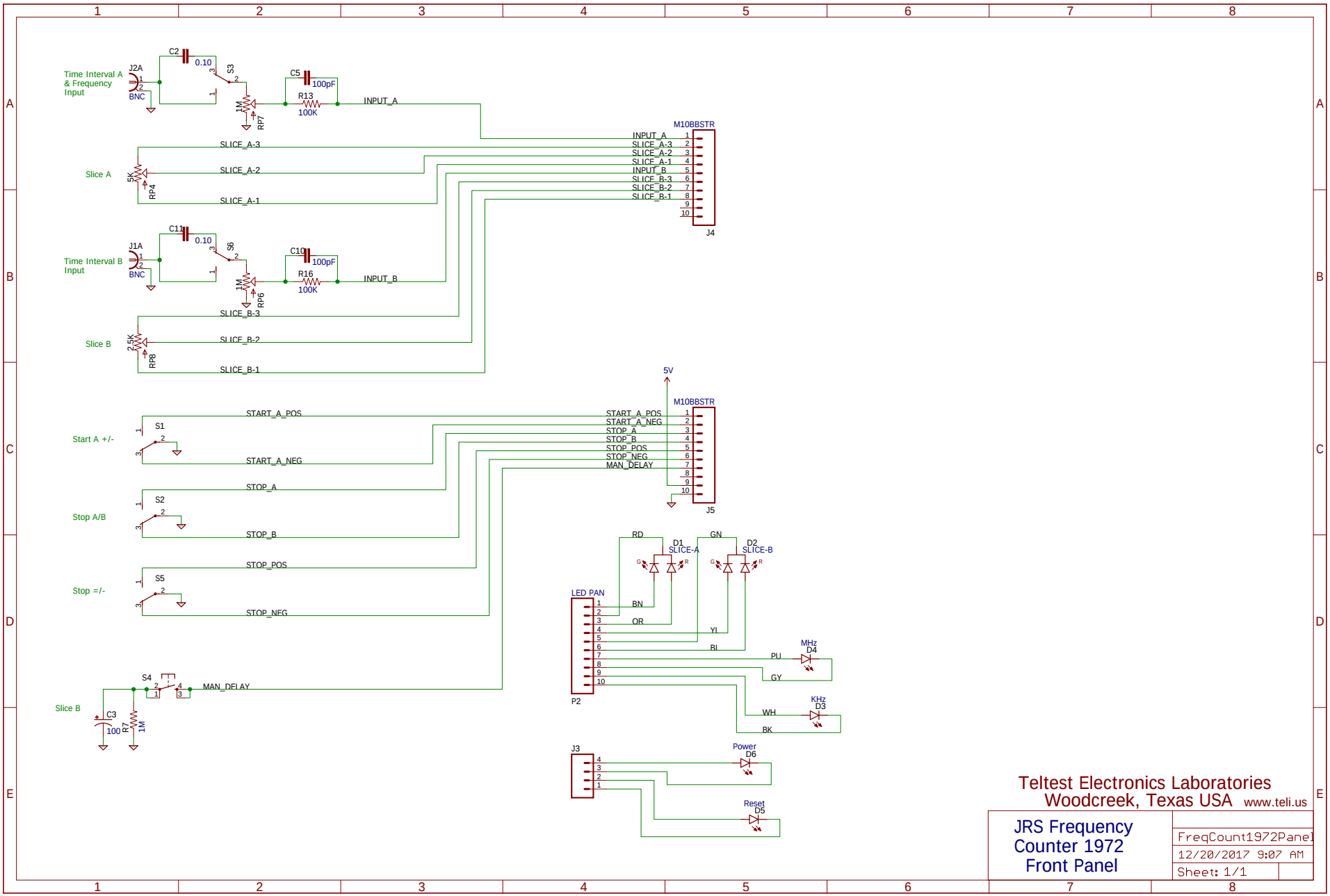
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J2A
BNC
C2
0.10
S3
1M
RP7
C5
100pF
R13
100K
INPUT_A
M10BBSTR
INPUT_A
SLICE_A-3
SLICE_A-2
SLICE_A-1
INPUT_B
SLICE_B-3
SLICE_B-2
SLICE_B-1
J4
Slice A
5K
RP4
SLICE_A-3
SLICE_A-2
SLICE_A-1
Time Interval B Input
J1A
BNC
C11
0.10
S6
1M
RP6
C10
100pF
R16
100K
INPUT_B
Slice B
2.5K
RP8
SLICE_B-3
SLICE_B-2
SLICE_B-1
5V
M10BBSTR
START_A_POS
START_A_NEG
STOP_A
STOP_B
STOP_POS
STOP_NEG
MAN_DELAY
J5
Start A +/-
S1
START_A_POS
START_A_NEG
Stop A/B
S2
STOP_A
STOP_B
Stop =/-
S5
STOP_POS
STOP_NEG
Slice B
S4
MAN_DELAY
C3
100
R7
1M
RD
GN
D1
SLICE-A
D2
SLICE-B
LED PAN
BN
OR
YI
BL
PU
GY
WH
BK
MHz
D4
KHz
D3
P2
J3
Power
D6
Reset
D5
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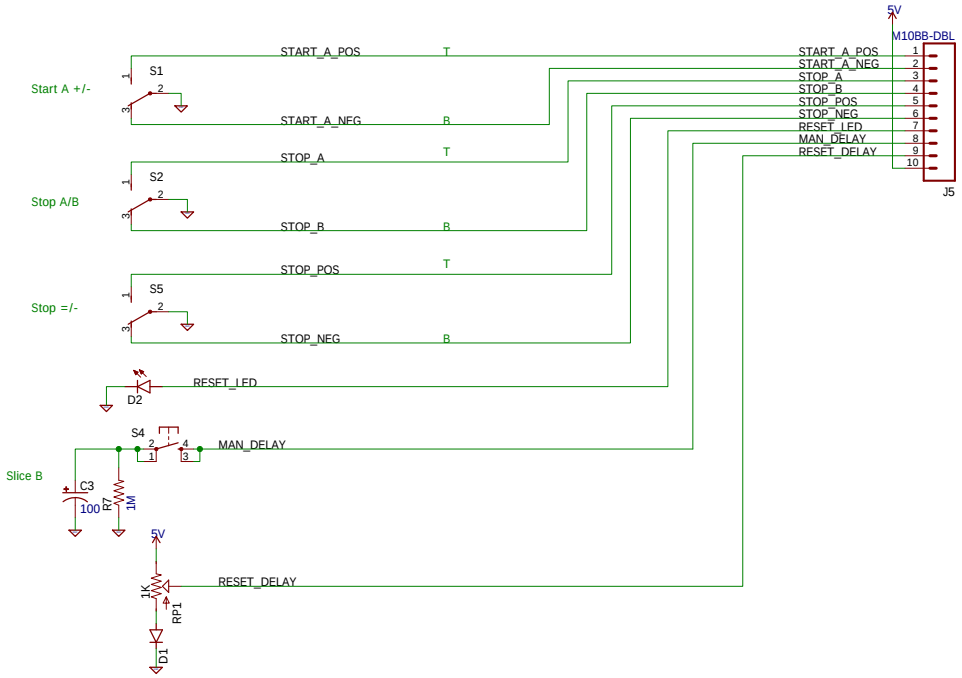

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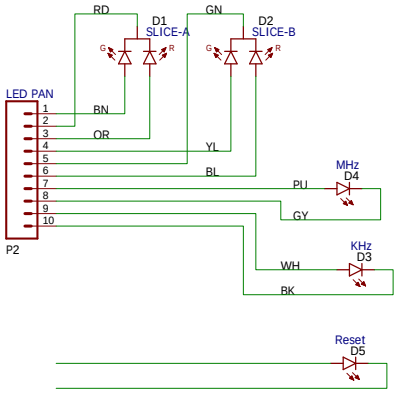

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Bell Laboratories

subject: A Battery-Operated Digital Frequency Counter and Time Interval Instrument - Case 21275-205

date: October 18, 1972

from: J. R. Satterwhite

ABSTRACT

A basic battery-operated frequency counter and time interval instrument has been designed and documented as a dinner hour project over the past several months. A breadboard of the unit has been constructed. The unit is capable of frequency measurements to 280 MHz and time interval measurements to 1000 sec. The maximum resolution in the time interval mode is 100 nsec.

The design of the instrument as constructed is discussed, and suggestions are given to decrease the power consumption.

Bell Laboratories

subject: A Battery-Operated Digital Frequency Counter and Time Interval Instrument - Case 21275-205

date: October 18, 1972

from: J. R. Satterwhite

MEMORANDUM FOR FILE

Introduction

This memorandum describes a battery-operated digital frequency counter and time interval instrument. This instrument was designed, constructed, and documented as a dinner hour project over the past several months. In our work, we have need of accurate lightweight battery-operated portable test equipment. This frequency counter and time interval instrument can help meet these needs.

General Description

The instrument readout as constructed consists of six 7 segment displays. It is capable of measuring frequencies from near DC to approximately 280 MHz and time intervals to 1000 seconds from either a single input or from two independent inputs. The basic clock frequency of the instrument is 10 MHz. The instrument in its present configuration consumes approximately seven watts of power; however, as will be discussed later, various configurations of the basic design are possible with greatly reduced power consumption, of course, at an increased expense.

The basic logic of the counter is TTL, primarily 74H series logic with some 74S series Schottky logic for the high speed input circuits. The input impedance of the instrument for time interval and frequency to approximately 80 MHz is 1 megohm shunted by approximately 20 pf to ground. The sensitivity of these two inputs is approximately 50 millivolts. Above 80 MHz, a prescaler is necessary and its input is capacitively coupled. The input impedance in the prescaler mode is approximately 50 ohms. Each frequency of the time base, 10 MHz by decades to 1 Hz, is available at the back panel of the unit.

The display readouts are of the incandescent direct view filament type and are of very low power consumption. The current requirement operating at 5 volts is approximately 5 milliamperes for each segment of the 7 segment display. This compares to approximately 35 milliamperes per segment for a LED readout of similar size. Power is supplied to the unit by Nicad batteries or from an AC power supply. Provision is made to display BCD information from another source simply by supplying the BCD information to a connector on the rear of the unit.

The display information can be presented in two modes. The first mode is with the display connected directly to the decade upcounters which accumulate the information. In this case, one observes the display as the counters count and the display time of resultant information can be substantially less than the total period involved, i.e., count period plus display interval. In the second mode, the display is connected to a storage register and the storage register is updated each time a new count result is available. In this configuration, one only sees the changes at the update. Leading zeroes are blanked in both modes.

The instrument is provided with an automatic recycling function whose period can be varied according to the operator's desires. By extending the period to infinity, the operator can manually reinitiate the counter by depressing a restart button. This allows a continually updated or a "read when desired" type of reading.

In the time interval mode, the measurement interval always starts from input A. The measurement interval may be terminated by either input A or input B. In each case of stop or start, the interval period may be initiated or terminated with either the positive going or the negative going edge of the waveform to be measured, that is, plus to plus, plus to minus, minus to minus, or minus to plus. Thereby all the parameters of a pulse train may be measured.

Each time the counter is reset; an LED on the front panel flashes indicating such. LED indicators also indicate the correct units associated with the function switch position. LED indicators also display the input data stream as a function of the input level control. If the LED is full off, the level control is below the signal. If the light is full brilliance, the level control is above the signal. In adjusting the level control, the LED is on but dim at the proper setting.

Circuit Description

First, the circuit, as constructed, will be described. Following that, readily available alternatives will be suggested. Implementation of these suggestions can, at increased expense, reduce the power consumption of the instrument.

Figure 1 is a logic diagram of the counter and display section of the instrument. First, we will look at the display circuit. The display circuit receives the binary coded decimal (BCD) information from either the decade counter shown or an outside source and is fed first to a 74157 which is an eight-line to four-line multiplexer. Therefore, either one set or the other set of the BCD information is outputted from this package. The output of the multiplexer is connected to a 7475 quad latch which is a storage register for the BCD information. The output of the storage register is then connected to a 7446 BCD to seven segment decoder. The seven segment information from the decoder is then fed to the seven segment display which displays the BCD information decimally.

The decade counter section (Figure 1) is made up of six 7490 decade counter units. The first counter unit is a high speed decade counter composed of two 74S112 dual JK flip flops. With the addition of a 74S00 gate, the 74S112's are connected as a decade counter. Following the high speed decade counter are five 7490 decade counters. Each decade counter's BCD output is connected to a display circuit. The counter and display sections have basically five inputs, the first is the input signal to be counted, the second is the reset, the third and fourth are store commands to store the information in the 7475 storage registers. The fifth input is information from the function switch for decimal point location.

Figure 2 is a logic diagram of the time base counter. It consists of eight 7490 decade counters connected in series. The counter is connected such that when it is reset, it is reset to the all nines state. The reason for this will be discussed later.

Figure 3 is an overall schematic and logic diagram of the instrument with the exception of the function switch. In the uppermost portion of the figure are the crystal oscillator (10.000 MHz) and the time base counter which

produce the frequencies from 1 MHz to 0.1 Hz. The output from the time base counter is connected to two 74151 eight-line to one-line multiplexers IC3 and IC4. The multiplexers are controlled by BCD connections on the function switch. The output of one multiplexer is used for the frequency function, the output of the other multiplexer is used for the time interval function. The output of the time interval multiplexer is also available at the back panel such as to provide 10 MHz through 1 Hz signals depending on the position of the function switch.

The general operation of the control logic is that first the decade counter is reset to an all zeroes state and the time base counter is reset to an all nines state. Following the reset, the counter counts until the end of count condition is satisfied, at that time either flip flop IC6B or IC5B goes to the Q high state and single shot IC13 is initiated. IC13 provides the delay between end of count and reset. The delay may be anywhere from infinity to a few hundred milliseconds. This delay is adjustable via the reset delay potentiometer on the front panel. When the delay times out, it initiates single shot IC14 which provides the reset pulse. IC6A and B are the control flip flops for the frequency counter function, and IC5A and B are the control flip flops for the time interval function.

The frequency counter time base is controlled by the output of the frequency multiplexer IC4 from the time base counter. The function switch determines which time base will be fed into the flip flops. Following the reset pulse, the first high going low signal from the multiplexer will set flip flop IC6A*. This enables the input pulse stream into the counter and display via gate IC2B. The input pulse stream comes to pin 12 of IC2B from the analog input circuitry. The output is then OR'ed through IC2C into the input to the decade counter. The counter enable signal (the Q output of IC6A) is connected to the J input of IC6B. Therefore, IC6B is enabled to flip on the next high going low signal from the multiplexer, the end of that time base period. When this condition takes place, IC6B flips and the counter enable is terminated via the Q output of IC6B which is OR'ed through IC8C, IC12A and IC2C to remove the input from the

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*For this reason, the time base counter is reset to the all nines state. In this way, one clock period after the reset pulse the frequency counter time base is initiated.

counter and display. This is done in this fashion such that when the count is enabled, the input stream to the counter will be low and can only go high with the presence of a signal transition. A condition could exist whereby the input signal was high and the application of the counter enable signal would cause the input to the counter to go low, therefore giving a false count. This is prevented by holding the input low. Now, if the counter enable is terminated in the same way that it begins, that is, by going low, it is possible to get a false count at the trailing end of the count enable period. This situation is prevented. At the trailing end of the count enable period, the input to the counter is carried high and held high, and therefore, a negative transition does not occur and a false count does not take place. The decade counter counts only negative going transitions. During the reset period, IC6A and 6B are reset restoring the low condition to the input to the decade counter.

The time interval flip flops IC5A and B operate in much the same manner. In this case, we have a separate start and stop signal. The signals come from the outside world. The first high going low transition on the start line following the reset period sets flip flop IC5A. This, then, enables IC12A pin 2 which allows the output of the time interval multiplexer from the time base counter to go to the input of the decade counter and display unit. The function switch selects the proper counting frequency from the time base counter. The Q output of IC5A is also connected to the J input to the IC5B. When a high going low transition occurs on the stop input to IC5B, it flips to the set state and via the Q output to IC8C the input to the decade counter is forced high and stays high, as with the frequency function. Again during the reset period IC5 is cleared. This forces the low condition back on the input to the decade counter ready for the next count condition. Therefore, in the time interval measurement, a standard frequency is counted for the time interval that is desired, resulting in the time of interest.

Next, we will look at the input circuit and will start with the time interval input B. The input comes in via a switch whereby AC or DC signals may be selected. The signal is fed to the gate of Q3 a junction FET, which is connected as a source follower. The output of the source follower is connected to the inverting input of IC1 which is a differential analog to TTL converter. The input signal is limited on the base of the FET by back to back diodes. The reference signal

for the other side of the differential analog to TTL converter noninverting input is fed from a similar junction FET connected as a source follower. On its gate is a reference potential which is adjustable from the front panel. This allows the operator to select the slicing point on the incoming signal. The output of the differential to analog converter is fed back to the noninverting input to yield positive feedback and form a hysteresis loop such that when the signal passes through the transition region, it is prevented from acting further on noise.

Next, we will look at the time interval A and frequency input. The operation of this circuit is identical to that of time interval B above with the exception that the FET source followers are followed by low impedance emitter followers prior to connection to the differential to analog converter IC1A. This allows a higher frequency response. The input B frequency response is in excess of 20 MHz. The time interval A and frequency input operate to 80 MHz. The output of the time interval A and frequency input is connected to high speed Schottky logic. The output of IC1A is then divided via IC2B to the time interval circuit and to IC2D for the frequency counter circuit. The frequency counter circuit is high speed Schottky logic and the time interval circuit is regular TTL. It is the output of IC2B, the frequency signal, which is allowed by the count enable pulse from flip flop IC6A to be counted by the decade counter.

The time interval A signal goes two places. First, to the start signal polarity gates which allow the selection of either starting on a positive or negative transition and second, to the stop selection gates where the stop function can be selected to be controlled by either A or B signal and then from control selection to the stop signal polarity gates. The stop signal may be either a positive or negative transition. For the start signal positive or negative transition, the signal and its inverse via IC10F are fed to an AND/OR Invert gate (AIO), and the selection takes place by enabling the AND on the signal or on its inverse as desired. Selection of the A or B signal is accomplished in the same manner and as is the stop positive or negative selection. The outputs of the AOI's IC11A and B are the stop and start signals which are fed to IC5A and B, which then control the time interval timing. The operator can therefore choose whether the counter is to stop on signal A or signal B and whether it is the stop and start on the positive or negative transition on the respective signals.

This allows one to use the frequency input to measure a period of incoming signal or one can measure the time difference between separate signals.

For high frequency signals above 80 MHz, a prescaler is necessary, and frequency counting to approximately 280 MHz is accomplished by a decade prescaler. The prescaler IC27 is a Fairchild 95H90 emitter coupled circuit, which has a built in analog to digital input circuit and comes complete in a single DIP package. The output of the prescaler is connected to the reference input for the frequency measurement allowing this input then to go into the main stream of the frequency measurement. The prescaler has power connected to it only in the prescale condition of the function switch.

The function switch layout is shown in Figure 4. Three decks of the switch are allotted to the time base multiplier select inputs. One deck on the switch selects the decimal point on the counter display for proper position. One deck of the switch lights LED's on the front panel to indicate whether the measurement is kHz or MHz, or seconds or milliseconds. Another deck is used for time interval frequency measurement selection. The last deck is used to apply power to the prescaler in the prescale position.

Figure 5 is a saturable core inverter which is used to provide the minus 5 volts for the input circuits. This allows operation from a single plus 5 volt battery. The counter may be operated from a 5 volt battery or from an AC power supply. The input power to the unit in this configuration is approximately 7 watts.

Suggestions for Reducing Power Consumption

The power consumption of the counter can be reduced in several ways. Each drop in power consumption almost certainly results in an increase in cost.

Figure 6 shows an alternate low power display circuit. Power consumption for this circuit is approximately 300 MW per decade while that for the more economical circuit already given is approximately 800 MW per decade. In the low power circuit, the 74L98 serves both the function of an eight line to four line multiplexer and storage register.

Power could also be reduced by replacing the second through the eighth stages of the time base counter with 74L90 decade counters. This would result in an approximate 900 MW saving.

If one is willing to sacrifice high frequency performance, a saving in power can be realized by making the time interval A and frequency input circuit identical to the time interval B input.

Accuracy

The accuracy of the instrument is of course dependent upon the clock. The clock circuit show has been measured to be stable to within ±50 Hz (±.0005%) over a period of two months. Long term measurements have not been made nor have precise temperature measurements. Gross temperature measurements indicate about a 150 Hz change in going from room temperature to 0° C.

More precise clocks are available which could operate from the units basic power at a significant increase in cost. If addition digits were displayed, such an investment might be justified.

Comments and Observations

After working with the constructed model, it has become obvious that it would be desirable to display more digits. It seems that eight would be much better and that ten would probably be ideal. It should be noted that this may be accomplished with the information given simply by adding the appropriate number of display circuits and possibly modifying some function switch connections. The control logic needs no change.

Time interval measurement of short pulses is hampered by a lack of resolution. A practical clock frequency upper limit is 10 MHz which limits the resolution to 100 nsec. For a 50 usec pulse this limits the reading to three significant figures.

Conclusions

A basic battery-operated frequency counter and time interval instrument has been designed. The design as constructed has been presented along with some suggestions to decrease the power consumption.

The writer feels that this has been a worthwhile and useful project.

J.R. Satterwhite

GC-4564-JRS-jfs

J. R. Satterwhite

Attachments
Figures 1 through 6

Copy to
See next page

Copy to (Continued)
Messrs. M. W. Bowker
R. J. Parker
W. S. Pesto
T. W. Robinson

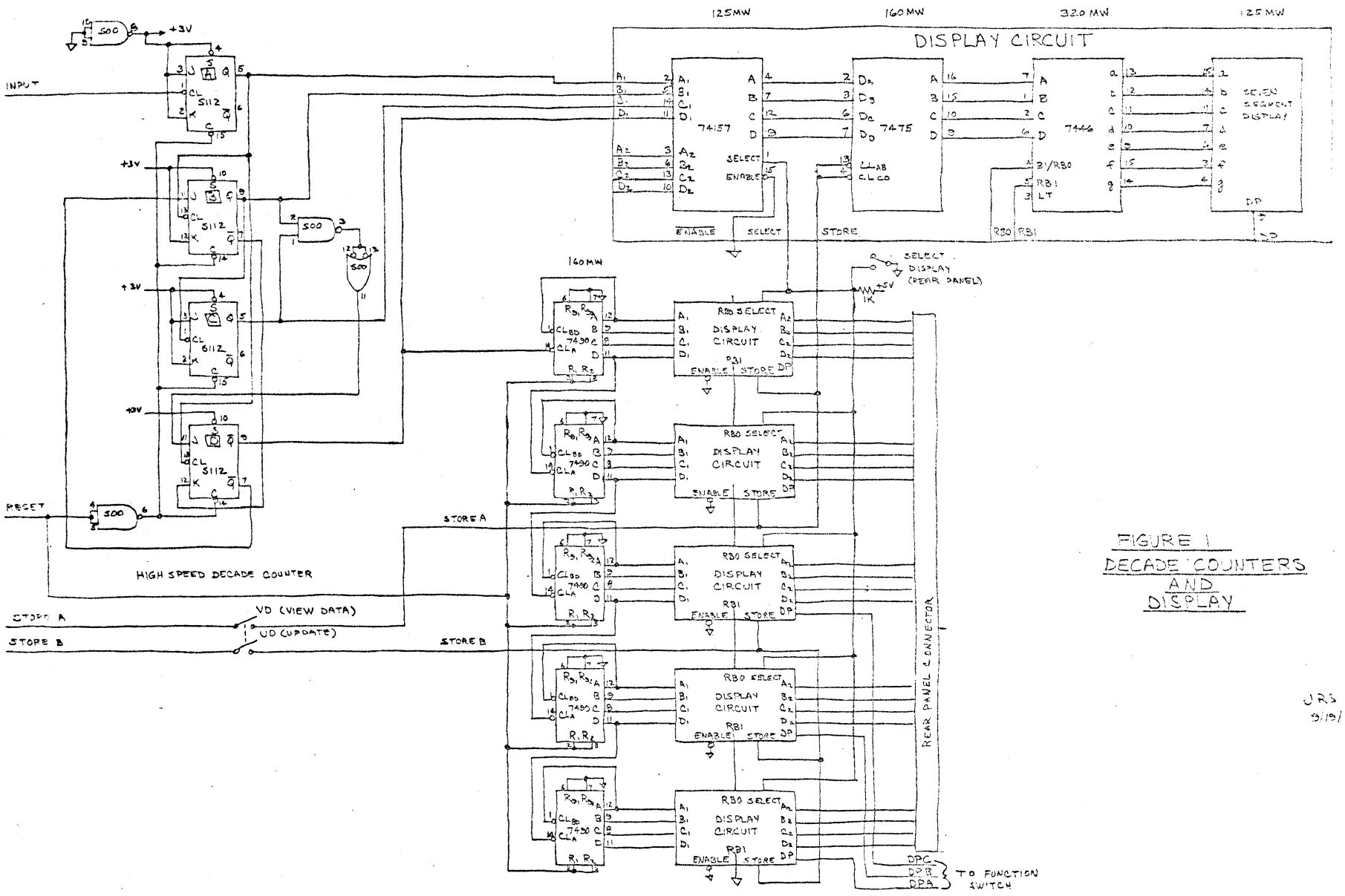

FIGURE 1
DECADE COUNTERS AND DISPLAY

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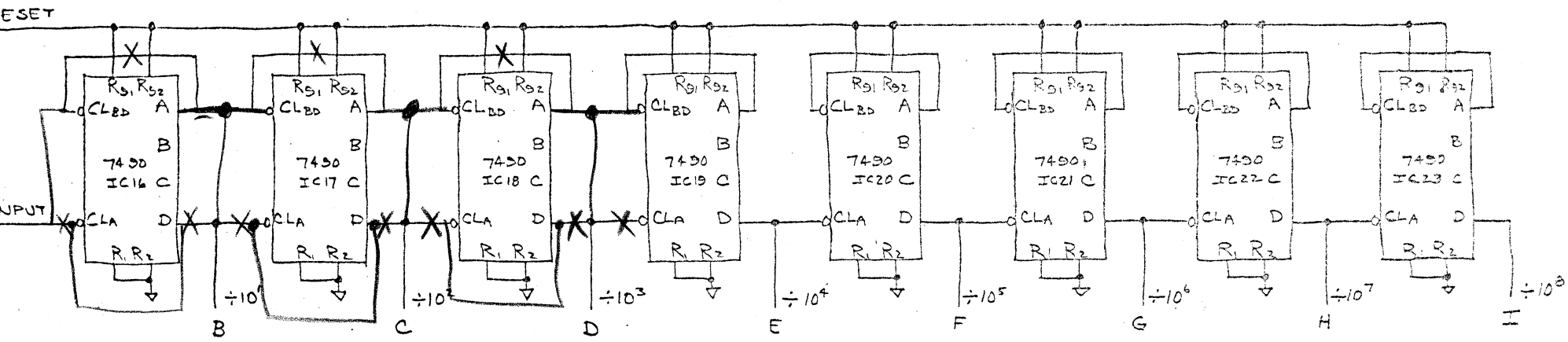

FIGURE 2
TIME BASE COUNTER

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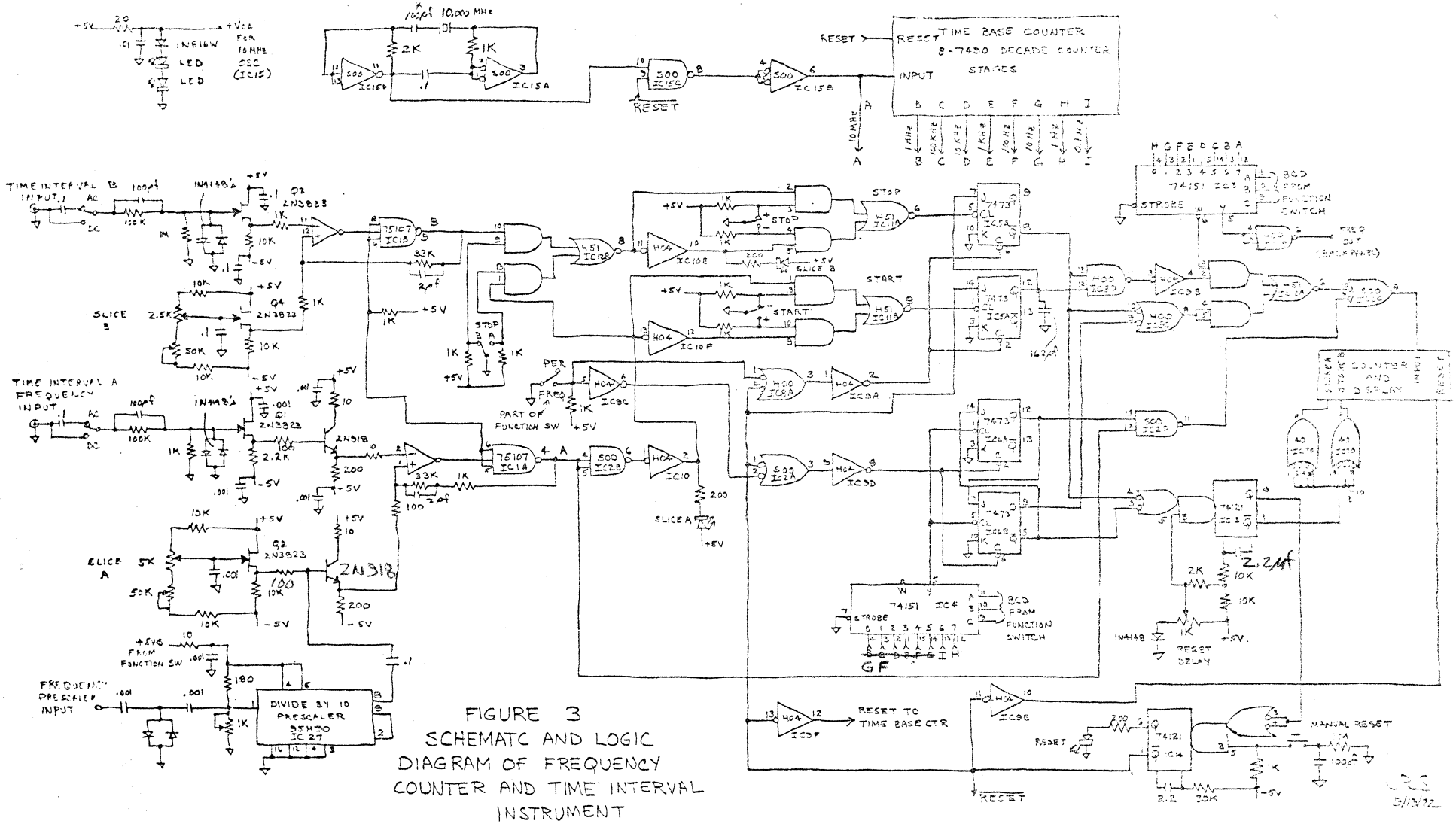

FIGURE 3
SCHEMATC AND LOGIC
DIAGRAM OF FREQUENCY
COUNTER AND TIME INTERVAL
INSTRUMENT

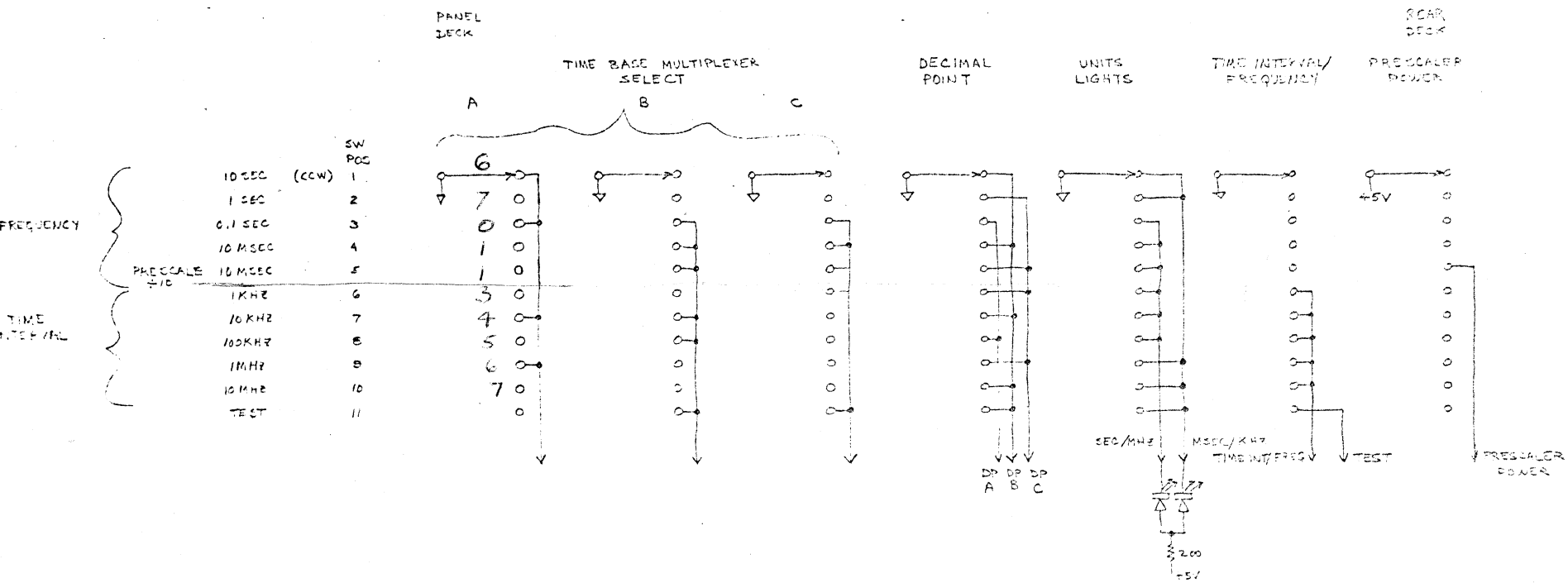

FIGURE 4
FUNCTION SWITCH

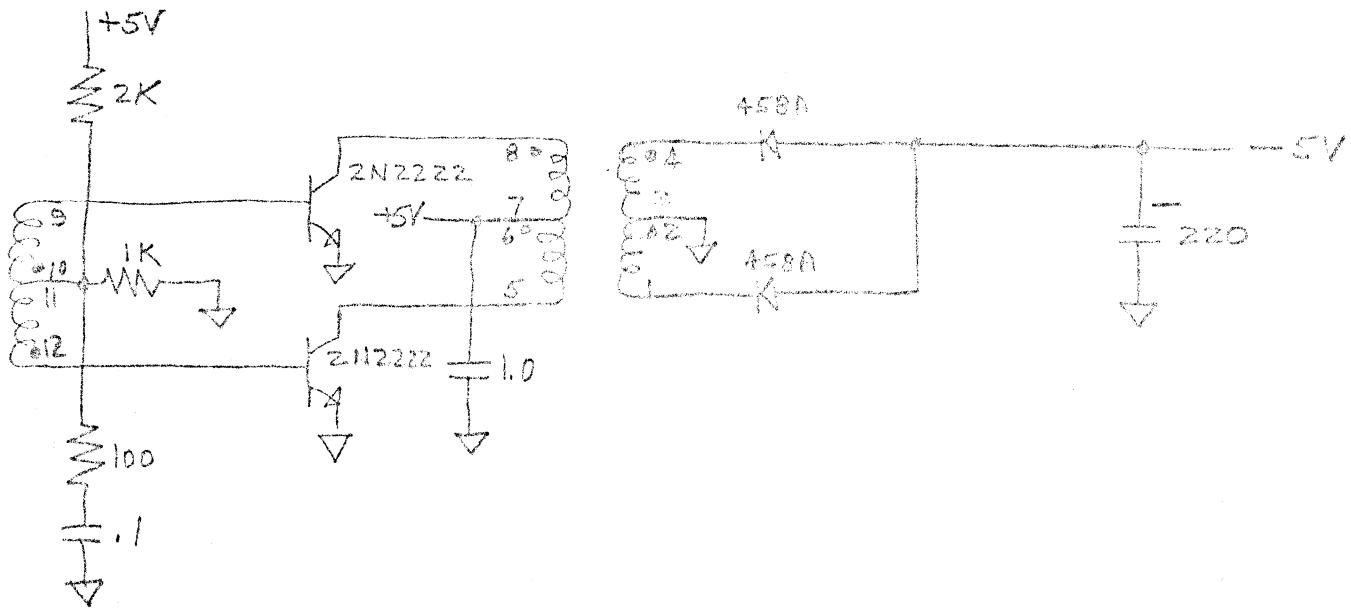

FIGURE 5
SATURABLE CORE INVERTER

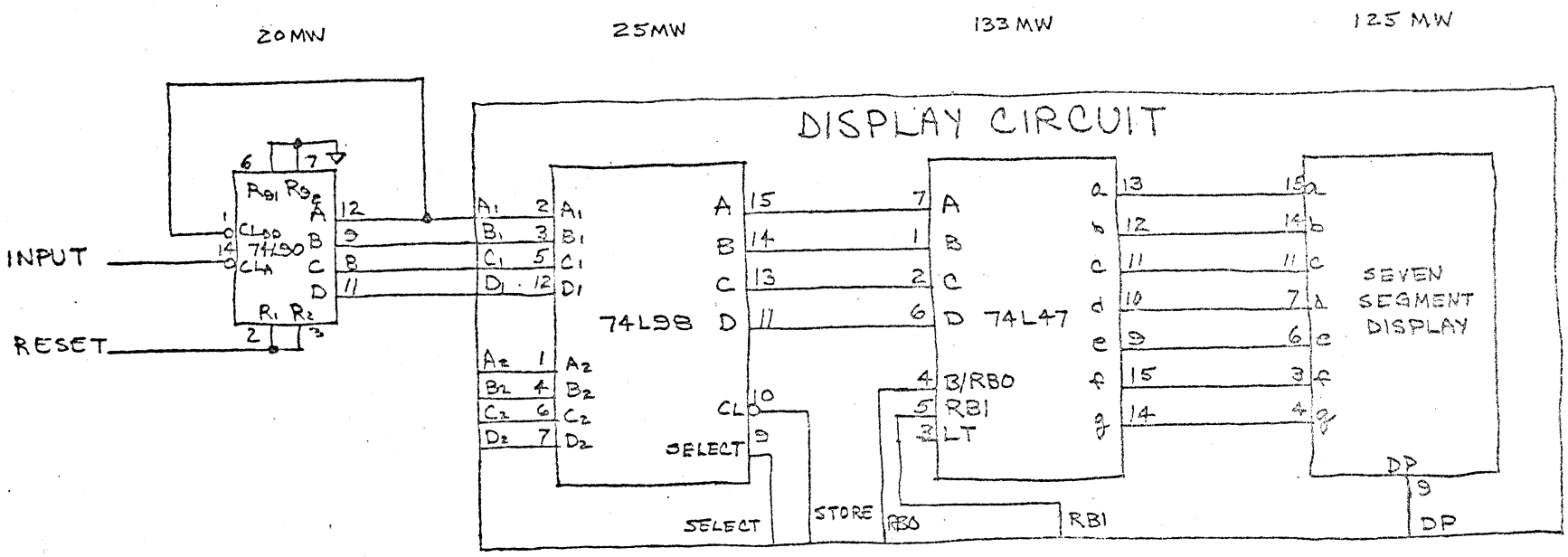

FIGURE 6
ALTERNATE LOW POWER
DISPLAY CIRCUIT

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